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TITLE: Asynchronous channel error mechanism

Detailed Description Text (3):
A computer system in accordance with the present invention consists generally, as shown in FIG. 1, of a central processing unit (CPU) 1, a virtual address translator (VAT) 2, an I/O channel 3, an addressable memory or main storage 5 and an I/O device adapter 4. Instructions fetched and executed by the CPU 1, as well as data and I/O commmands, are all stored in the addressable memory or main storage 5. These various elements are connected to each other directly and indirectly by means of various lines and busses, which will be discussed in greater detail below and are identified in FIG. 1. The system would typically include a plurality of I/O adapters, but, for simplicity only one is shown in FIG. 1. It will also be understood that the I/O adapter 4 is connected to one or more I/O devices, e.g., magnetic tape drive, magnetic disk drive, not shown here. The I/O adapter 4 is the interface between the channel 3 and the I/O devices. For purposes of the present discussion, the relationship between an I/O adapter and its attached I/O device need not be considered in detail, and generally only the channel-adapter relationship will be described.